

Lab #1

Combination Logic Using VHDL

DATES OF EXPERIMENTATION

October 28, 2019

November 4, 2019

DATE OF LAB REPORT

November 11, 2019

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Rochester Institute of Technology
CPET233: Digital System Design Lab
Lab Section: 01

Lab #1: Combination Logic using VHDL

ABSTRACT

The abstract should be limited to as few words as possible (about 1/2 page). It should clearly convey to the reader what the objective of the laboratory was, how the objective was met and what the overall results were. This statement should be completely self-containing and may not reference any other section of the documentation. This section must be typed and be written in the 3rd person / past tense.

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LAB REQUIREMENTS SUMMARY

Describe the requirements for the circuit that was designed for the lab and what its functionality should be. Define any special modifications you may have made to the experiment. Define the inputs and outputs in detail. Use figures and tables to summarize the requirements. Describe any equipment that is required to perform the experiment. Start with the information provided on the lab assignment sheet and expand on it. Do not reference the lab assignment sheet. This section should be past tense.

Figure I: Block Diagram

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RESULTS AND DISCUSSION

Discuss what your results were and what the results mean. Provide the important data addressing your objectives and hypotheses. Summarize as much as possible. This is where you tell the reader what all these measurements (outputs) mean. Do not assume that just looking at the data reveals intuitively obvious conclusions. Tell the reader exactly what the results mean. For example, "The second row in Table II contains...There is a consistent trend; the duty cycle of the output was controlled by the... the amplitude/frequency was directly related to..." **Refer to source code and waveforms here.**

Figure II: Circuit Diagram

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CONCLUSION

This is short technical summary of your design where you wrap up the report. If you had to do the design over again, would change the design? Are there design issues or pitfall that others should watch out fall?

APPENDIX A: SCHEMATIC DIAGRAM

APPENDIX B: SOURCE CODE

APPENDIX C: TIMING DIAGRAMS/WAVEFORMS