Homework #3 – Due 9/18/19
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1. Consider the 4-input 1-output function Prime. The output is a 1 if the binary number formed by the 4 inputs is a prime number.
   a. Complete the truth table for Prime. Remember 0 and 1 are not prime numbers, but 2 is. Submit the truth table.

A	B	C	D	Prime
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

   b. Write the VHDL (entity and architecture) for prime. This module should have four inputs (A, B, C, D) and four outputs (prime_sel, prime_cond, prime_case, prime_if). In the architecture write the code for prime four different ways (selected signal assignment, conditional signal assignment, case statement and if statement) and drive the corresponding output with each. Submit the code.
   c. Simulate the circuit using waveforms and verify the outputs are all the same and correct. Submit the waveform.
   d. Recompile with equation generation turned one. Examine the equations and comment on your observations. Submit the four equations and your observations.

2. Textbook exercise 5.9 (page 146)

3. Write sixteen **constants** for the 7-segment display to display the hex digits (0-9, a-f). Use these constants in a vhdl code that has a 4-bit std_logic_vector input and a 7-bit std_logic_vector output. The output should be assigned the

appropriate constant to display the hex equivalent of the input. Use a case statement in the VHDL. Submit the code.

IN(3)	IN(2)	IN(1)	IN(0)	Hex
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	b
1	1	0	0	C
1	1	0	1	d
1	1	1	0	E
1	1	1	1	F