Homework #6 – Due 10/9/19
Please submit a hard copy or put in the Dropbox in MyCourses

1. Consider a circuit that has two 3-bit inputs (A(2 downto 0), B(2 downto 0)) and three 1-bit outputs (AltB, AgtB, AeqB). The circuit does an unsigned comparison of A and B and sets the appropriate output to 1; AltB for A less than B, Agt B for A greater than B and AeqB for A equal to B. Write the VHDL for this comparator circuit keeping in mind the following:
    - Use the STD_LOGIC_VECTOR data type for the inputs in the entity, but the UNSIGNED data type internally
    - Ensure there is only 1 output per process
    - Verify there are no latch warnings. Submit the code to dropbox.

2. Using the testbench from lab4 as a guide, create a testbench to simulate the comparator for all possible input combinations. Pay particular attention to the loop statement. Refer to the end of the lecture 6 for an explanation of the loop. Submit the testbench code.

3. Use Modelsim to simulate the comparator circuit. Change the radix of A and B to unsigned and scale the waveforms such that they are readable. Visually inspect the waveforms to verify correct operation. You may have to take several screen shots to include the entire simulation in a readable format. Submit the waveforms.