# Exam 2 Practice Problems

# Announcements

- HW #7 due Friday
  - This is with new homework groups
- Wed and Fri labs are working on lab 7
- Exam on Monday 10/21

# Exam #2 Study Jam

Saturday October 19th

12 noon - 4 pm

Golisano 1360 (ESD lab)

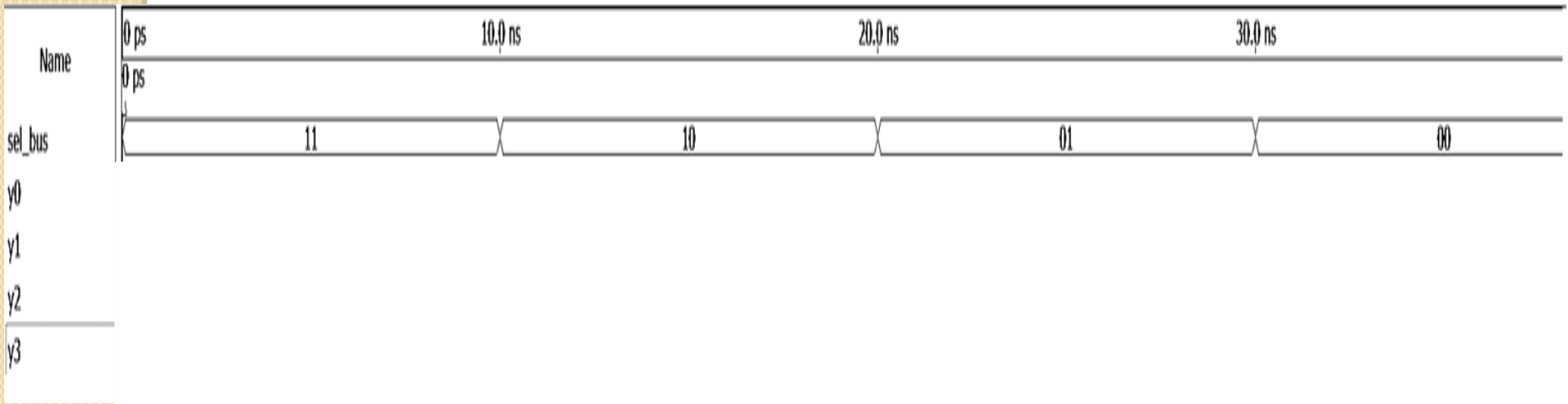
Bring questions

- Write the entity and architecture for a priority encoder with the following requirements:
  - Eight 1-bit inputs : I0 – I7
  - One 3-bit output: num_out
  - Use the following table

| Active Input | Num_out | Priority |
|---|---|---|
| I7 | 111 | 1st highest priority |
| I6 | 110 | |
| I5 | 101 | |
| I4 | 100 | |
| I3 | 011 | |
| I2 | 010 | |
| I1 | 001 | |
| I0 | 000 | 8th lowest priority |

# Complete the output waves for the decode2to4 architecture below.

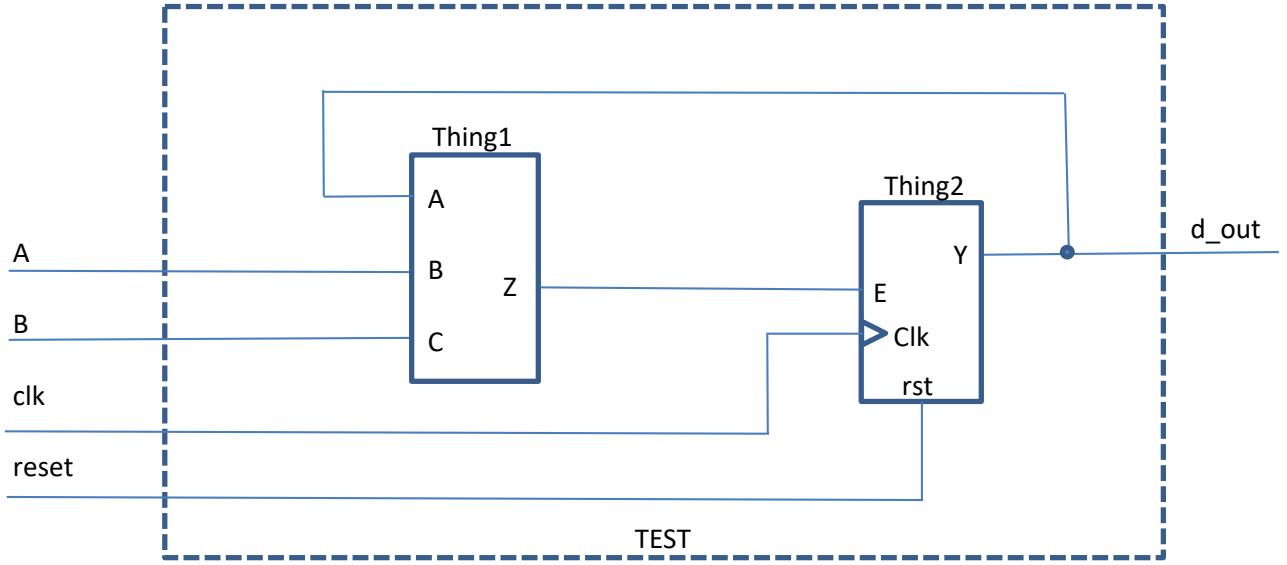
```
ARCHITECTURE behave OF decode2to4 IS

  signal sel_bus   : std_logic_vector(1 downto 0);
  signal Y_bus     : std_logic_vector(3 downto 0);

  BEGIN

     sel_bus <= s1 & s0;
     y0 <= Y_bus(0);
     y1 <= Y_bus(1);
     y2 <= Y_bus(2);
     y3 <= Y_bus(3);

     WITH sel_bus SELECT
        Y_bus <= "0001" WHEN "00",
                 "0010" WHEN "01",
                 "0100" WHEN "10",
                 "1000" WHEN OTHERS;
  END behave;
```



Rewrite the following mux architecture as a case statement

```
ARCHITECTURE behavioral OF mux IS
            SIGNAL selects: STD_LOGIC_VECTOR(1 DOWNTO 0);
BEGIN
          selects <= s1 & s0;
          output <= A when (selects = “00”) ELSE
                        B when (selects = “01”) ELSE
                        C when (selects = “10”) ELSE
                        D;
END behavioral;
```

# Complete the *STRUCTURAL* (hierarchical) VHDL model below. The component declarations for the two components are already given




```
ENTITY test IS
   PORT (A, B, reset, clk :  IN  STD_LOGIC;
            d_out             : OUT STD_LOGIC);
end test;

ARCHITECTURE structural OF test IS

COMPONENT Thing2 IS
    PORT(E, rst, clk     : IN STD_LOGIC;
            Y               : OUT STD_LOGIC);
    END COMPONENT;

COMPONENT Thing1 IS
    PORT(A, B, C  : IN STD_LOGIC;
            Z          : OUT STD_LOGIC);
    END COMPONENT;
```