CPET-233 Exam #2

Monday, October 21, 2019

In Class

Closed book ~ Closed Notes ~ No Calculators

Book sections covered on this exam:

Ch. 3 sections 7 & 18, Ch. 5 section 7

Ch. 8 section 3

Lectures covered:

Lecture 7 – Lecture 10.5

Homework covered:

HW #4 – HW #7

Labs covered:

Lab 4 – Lab 6

All material from exam 1

Lecture 7 –

- Understand the difference between std_logic_vector and integer in terms of synthesis.
- Understand how negative numbers are represented internally. Be able to convert a signed binary number to its decimal equivalence and how to negate a number. Know the range of possible values for an n-bit signed number and n-bit unsigned number.
- Understand what casting is and how to cast between std_logic_vector, signed and unsigned.
- Know the rules of VHDL addition, subtraction, multiplication and division.
- Be able to sign extend to create operands that are the correct length for the given operation.
- Know what an ALU is and where one can be found.

Lecture 8 – this lecture is very important. It's a summary of some very important topics.

- Know which signals go in a sensitivity list
- Understand when signals are assigned in a process and why the following code will not work as expected:

```
PROCESS(a_unsign, b_unsign)
    BEGIN
        a_unsign <= unsigned(a);
        b_unsign <= unsigned(b);
    if (a_unsign < b_unsign) then
        altb <= '1';
   else
        altb <= '0';
   end if;
end process;
```

- Understand how to write case and if/then/else statements so that a latch is not inferred and what is meant by one output per process
- Know what it means that an output port cannot be read and how to get around that restriction
- Know how to create a vector with concatenation and how to access individual bits of a vector
- Be comfortable with the parts of a test bench and how a test bench relates to the module being tested

Lecture 9 and 9.5 -

- Understand what is meant by hierarchical design and advantages of using it
- Know what a component is and how to declare it in an architecture
- Know how to write a structural architecture with components
- Know what a port map is and the syntax for one
- Review the example codes for hierarchy that are posted in MyCourses

Lecture 10 -

- Be able to identify what a comparator, decoder, encoder, multiplexer and code converter all do.
- Understand the relationship between number of inputs, outputs and selects for decoders, encoders and multiplexers
- Understand how the VHDL is written to implement each of the above
- Understand what a priority encoder is and how priority is determined

Lecture 10.5

- Be sure you can answer all of these questions