



CPET-233 Digital Systems Design Fall 2019

Homework #12 – Due 12/4/19

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1. A decoder is a circuit that in which one and only one output can be active at a time. The active output is determined by the decoder's select inputs. The table below is for a 3-to-8 decoder. The number of outputs is equal to $2^{\text{# of inputs}}$.

	Input			Output							
	2^2	2^1	2^0	0	1	2	3	4	5	6	7
Note: The selected output goes HIGH.	0	0	0	1	0	0	0	0	0	0	0
	0	0	1	0	1	0	0	0	0	0	0
	0	1	0	0	0	1	0	0	0	0	0
	0	1	1	0	0	0	1	0	0	0	0
	1	0	0	0	0	0	0	1	0	0	0
	1	0	1	0	0	0	0	0	1	0	0
	1	1	0	0	0	0	0	0	0	1	0
	1	1	1	0	0	0	0	0	0	0	1

Create a generic decoder in which the generic constant is the width of the input select bus. Both the input and outputs should be type `std_logic_vector`. You will have to use exponents, which are expressed with **, to set the width of the output bus.

2. Modify the universal shift register of HW #9 to make it generic length. Be sure to address any feedback you may have received on the original design.
3. Textbook exercise 8.8 (page 220). Include your compilation report showing the number of registers. You do not have to simulate.
4. Textbook exercise 6.6 (page 174)
5. Textbook exercise 6.7 (page 174)