

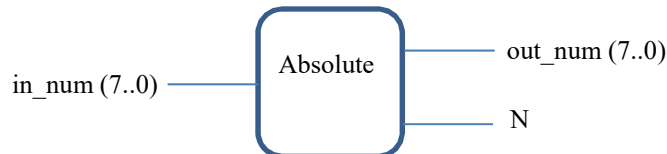


CPET-233 Digital Systems Design Fall 2019

Homework #5 – Due 10/02/19

Please submit a hard copy or put in the Dropbox in MyCourses

1. Textbook exercise 5.17 and 5.18. Submit both of the program codes.
2. Create a VHDL module (entity and architecture) to find the absolute value of a number.



In_num and out_num are 8-bit std_logic_vectors and N is a std_logic. The code should determine if in_num is positive or negative (by looking at in_num(7)). If the number is positive, out_num <= in_num and N is 0. If the number is negative, out_num is the 2's complement of in_num and N is 1.

3. Create a VHDL module for an adder/subtractor. The module has two 8-bit std_logic_vector inputs (A and B) and a std_logic input (A_S). A_S equals 0 for addition and 1 for subtraction. There is also an output called sum (remember sum needs to be 9 bits). You may not use – for the subtraction operation. To achieve A-B you should add the 2's complement of B to A.
4. Use the waveform simulator (or Modelsim if you would like) to simulate the following operations in your adder from question 3:

E + 4

7 + 6

0B + 17

23 + C5

DA + 22

F – 4

6 – 2

A3 – 18

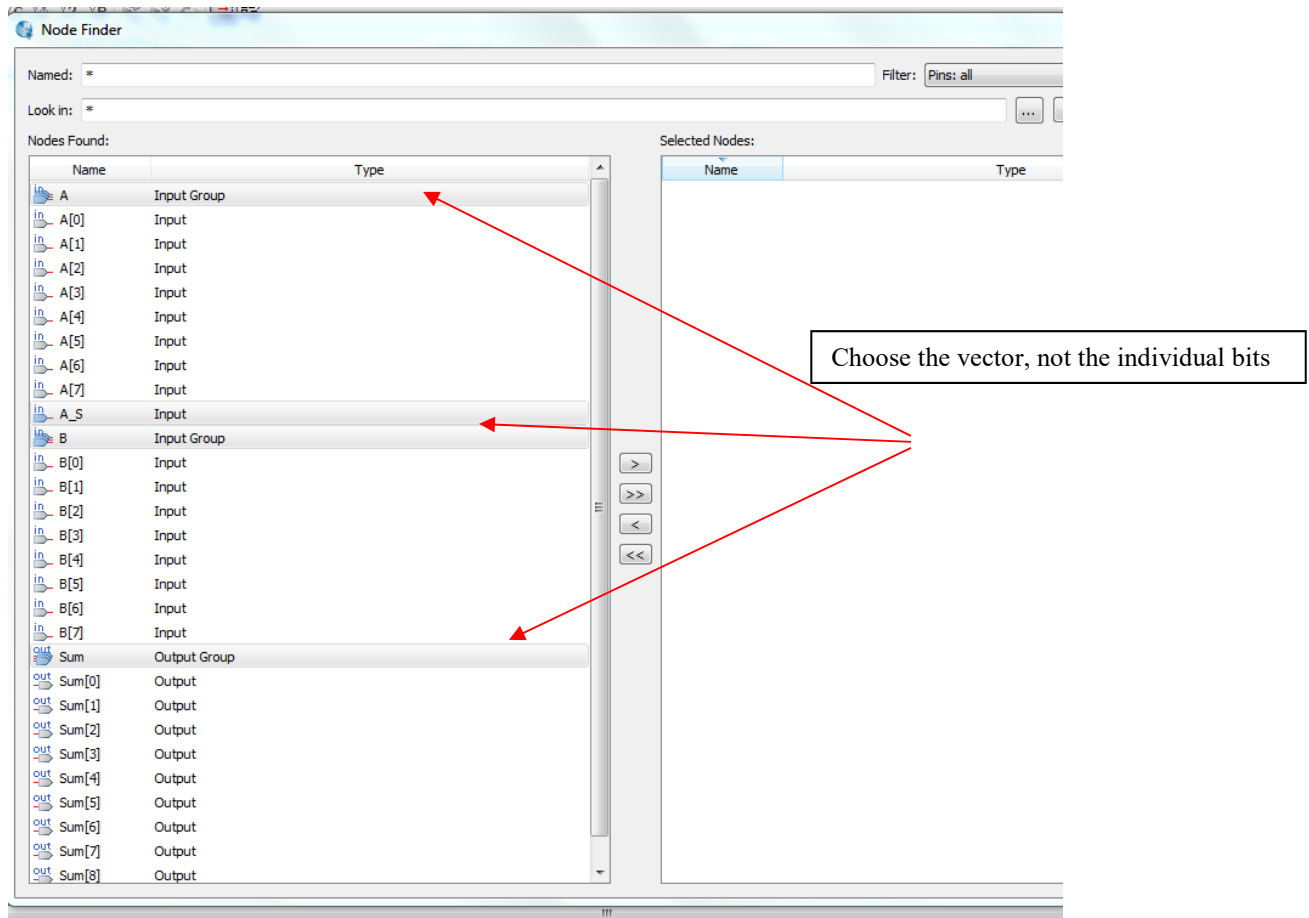
2D – 09

19 - 5C

To make things simpler, in the node finder, add the vectors to the waveform instead of the individual bits as shown below:



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- In the waveform window, set the end time to 100 ns.
- A_S should be low for the first 50 ns and high for the last 50 ns.
- To put a specific value on A or B, highlight a 10 ns span (as shown below). Then click on the ? on the toolbar. In the popup box change the radix to hexadecimal and then type in the value.
- Repeat this for all 10 problems

