Homework #8 – Due 10/30/19
Please submit a hard copy or put in the Dropbox in MyCourses

1. What are the differences between synchronous and asynchronous inputs to a memory element?

2. Why is D not needed in the process sensitivity list for a DFF?

3. What is the advantage of a flip-flop with an enable input?

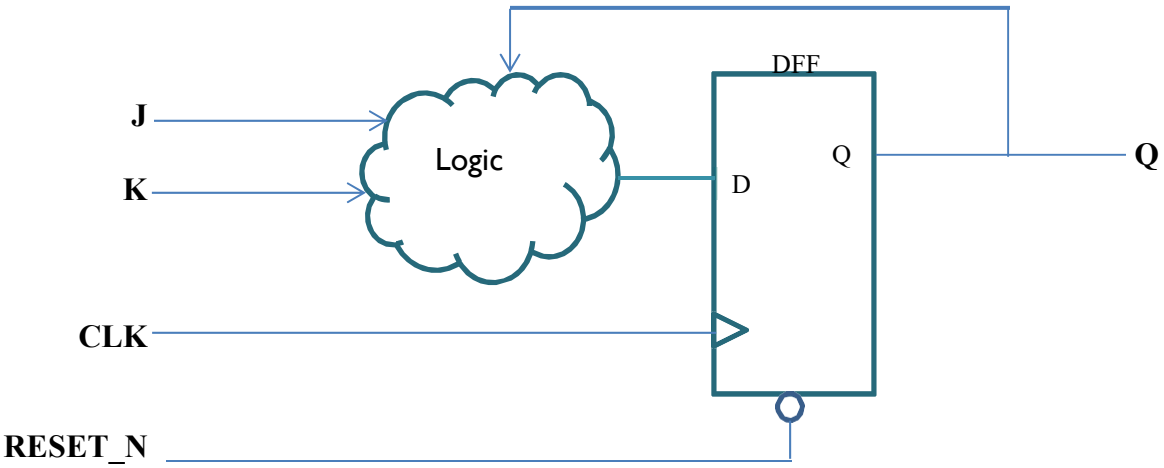
4. Write the entity and architecture for a DFF with a synchronous reset. After compiling, choose Tools > Netlist Viewers > RTL Viewer. Take a screen shot. Now change the architecture to make the reset asynchronous. Compile, view the RTL and take a screen shot. Looking at the two screen shots, what are the differences? Do you think the flip flop primitive built into the logic elements of the Cyclone V FPGA has a synchronous or an asynchronous reset? Why? Submit the screen shots and the answers to the questions.

5. Enter the code below into Quartus and compile it. Search the warnings. What do you see? View your results in the RTL Viewer. Take a screen shot and submit.

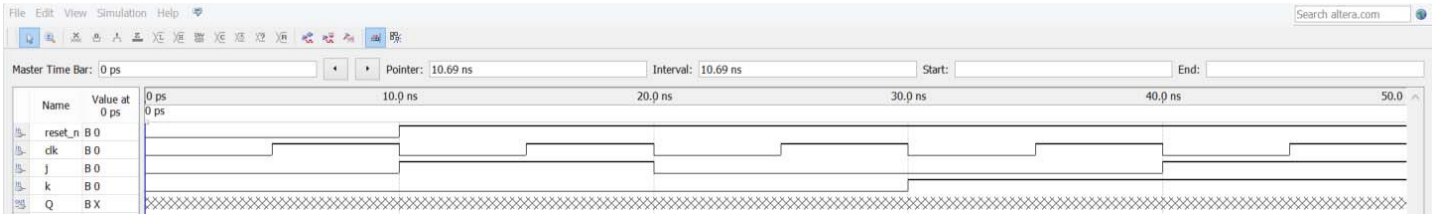
```
mux: PROCESS (sela,selb, a, b)
     BEGIN
        IF (sela = '1') THEN
            y <= a;
        ELSIF (selb = '1') THEN
            y <= b;
        END IF;
END PROCESS mux;
```

6. Create a JKFF from a DFF and additional logic. Start with one of the DFFs from Question 4 as a component and build other logic around it to implement the following truth table. Submit your code.

J	K	CLK	Q
0	0	↑	No change
0	1	↑	0
1	0	↑	1
1	1	↑	toggle



7. Use the Quartus waveform editor to create the following input waveform



Simulate your flip flop to verify its operation. Submit the final waveform.