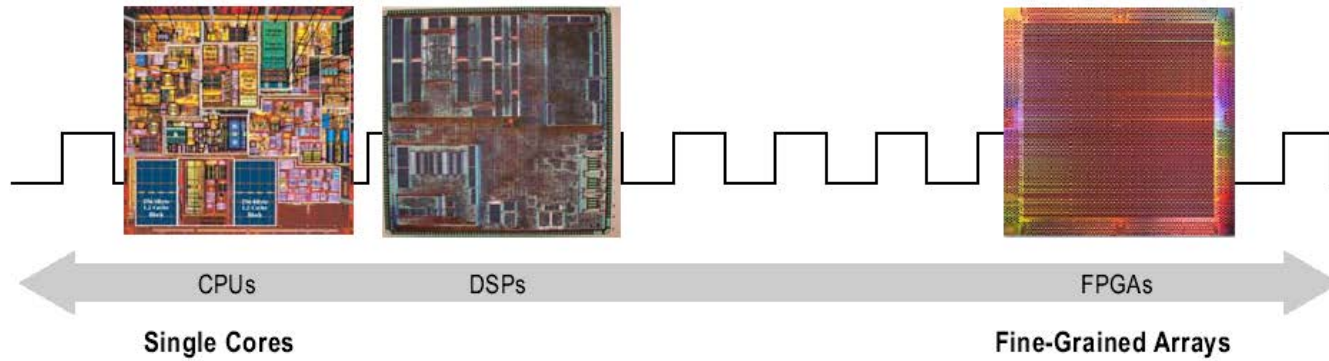
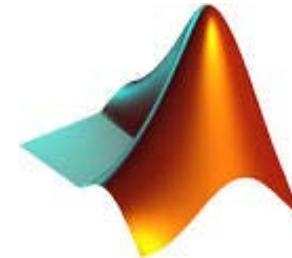
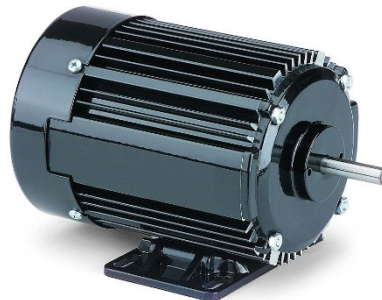


# SoC FPGA?



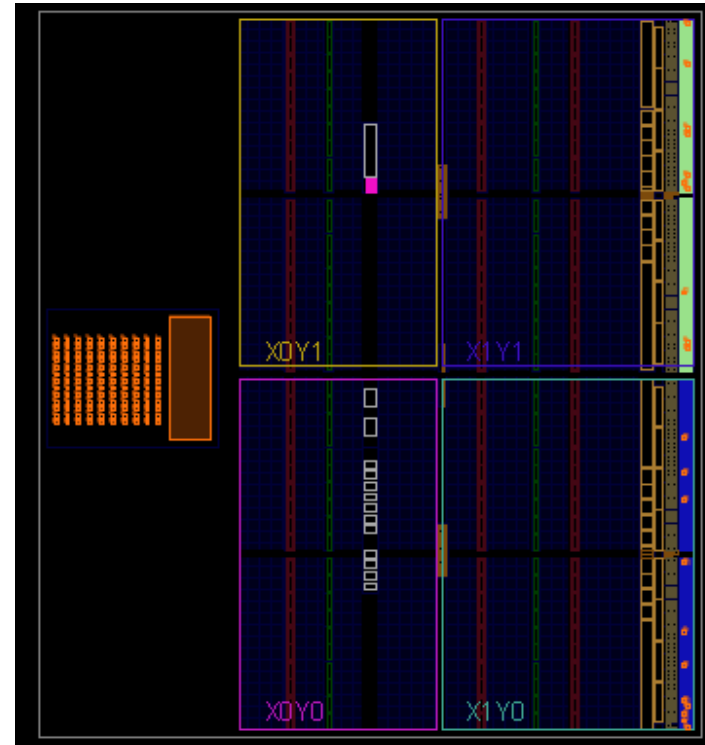
$$\text{SoC} = \text{CPU} + \text{FPGA}$$



OpenCL

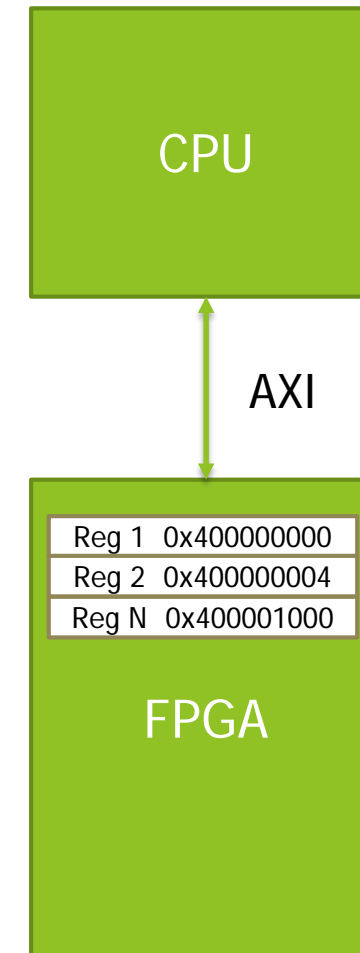
# SoC FPGA Architectures

- ▶ What is an SoC FPGA?
  - ▶ Fully Featured ARM Processor
  - ▶ Programmable Logic Fabric
- ▶ Why SoC?
  - ▶ Reduce Board Space and Development Time
  - ▶ Increased System Flexibility
  - ▶ Configurable FPGA/CPU Interconnect
  - ▶ Integrated Development Tool Flow
  - ▶ Open Source Software Ecosystem
- ▶ Xilinx Zynq-7000
  - ▶ 1 GHz Dualcore ARM® Cortex™-A9
- ▶ Altera SoC
  - ▶ 1 GHz Dualcore ARM® Cortex™-A9
- ▶ Microsemi Smart Fusion 2
  - ▶ 166 megahertz (MHz) ARM ® Cortex™-M3 processor



# Advanced eXtensible Interface [AXI]

- ▶ Background
  - ▶ Advanced Microcontroller Bus Architecture [AMBA]
  - ▶ AXI is Third Generation of AMBA
  - ▶ Introduced by ARM in 1996
- ▶ Xilinx Zynq SoC FPGA/CPU Interconnect
  - ▶ AXI4 - Address Followed by up to 256 Data Words
  - ▶ AXI-Lite - Single Address, Single Word
  - ▶ AXI-Stream - Unlimited Burst Transfers [non-memory mapped]
- ▶ Communicating Between FPGA and CPU
  - ▶ CPU
    - ▶ Bare Metal => FPGA registers accessible via global memory map
    - ▶ Linux => FPGA registers accessible via /dev/mem
  - ▶ FPGA
    - ▶ Processor values accessible via registers



Advanced eXtensible Interface [AXI]

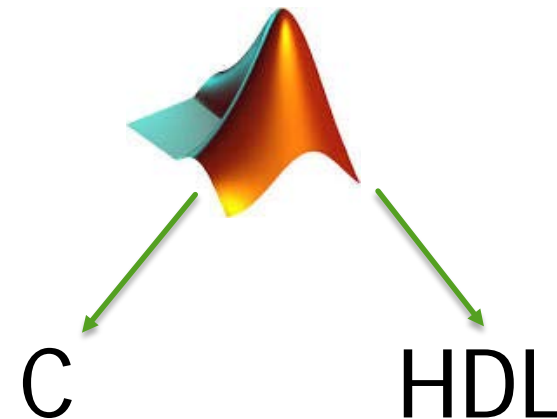
# Xilinx Zynq SoC FPGAs

	Zynq UltraScale + MPSoC	Zynq - 7000
Process Node	16 nm FinFET	28 nm
Application Core	Quadcore ARM® Cortex™-A53 MPCore™ up to 1.3GHz	Dualcore ARM® Cortex™- A9 MPCore™ up to 1GHz
Real-Time Core	Dual ARM® Cortex™-R5 MPCore™ up to 600MHz	-
GPU	Mali™-400MP up to 466MHz	-
High Speed Connectivity	2x USB 3.0, SATA 3.0, DisplayPort, 4x Tri-mode Gigabit Ethernet, PCIe Gen2x4	-
Logic Cells (K)	920 [~13.6 M]	444 [~6.6 M]
Block Ram	4.4 MB	3 MB
DSP Slices	3528	2020
UltraRAM	16 MB	-

# Algorithm Partitioning

Solution	Execution Speed	Determinism	Design Method
ARM Processor	High	Moderate	C
Soft Processor	Moderate	Moderate/High	C
HDL State-Machine	Very High	Very High	HDL

- ▶ Compile Time
- ▶ Floating/Fixed Point Implementation
- ▶ Algorithm Sizing
- ▶ Verification Methods
- ▶ Expandability
- ▶ Several Companies Offer IP for SoC FPGAs



kHz Loops -> CPU, MHz Loops -> FPGA