Hardware Description Languages
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Homework #4
Due 12-11-23

1. Download the pipeline.zip file and simulate it in Modelsim.

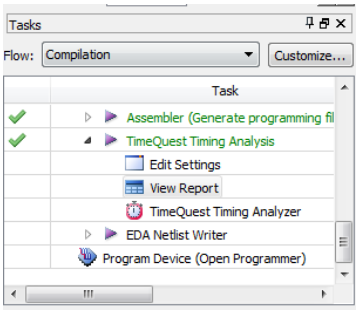
2. The value 1 is being added to the signal ‘a’ every 5 clocks and the ‘result’ signal contains ‘a’ raised to the power of 3.

3. How many clocks does it take to get the result after ‘a’ is updated? [1 pt]

4. Compile the project by clicking on the ‘compile’ batch routine in the HW folder.

5. Open Quartus by clicking on the pipeline project file located in the HW/project folder

6. In the Tasks window, click on ‘View Report’



7. In the Table of Contents, notice that some of the reports are in red. These are constraints that were not met.

8. Record f_{max} along with various time constraints that were not met. What is $f_{max.}$? [1 pt]

9. Question: What does negative slack mean? [1 pt]

10. Modify the pipeline flag by setting it to true in the pipeline.vhd file.

    a. constant PIPELINE_FLAG : boolean := true;

11. Re-simulate the design in Modelsim. How many clocks does it take to get the result after ‘a’ is updated? [1 pt]

12. Recompile the project, open the Quartus project, and record the new $f_{max.}$ [1 pt]

13. Discuss why the f_{max} is different between the designs and draw the datapath for each design from ‘a’ to ‘result’ [5 pt]